• **Location**

The symposium will be held on the University of Southampton’s Highfield Campus in the Hartley Suite, Building 38. Further information: [https://maps.southampton.ac.uk/](https://maps.southampton.ac.uk/)

• **Welcome Reception**

We kindly invite all participants to the Welcome Reception on Monday, September 2\(^{nd}\), at 6:00 pm, that will be held the Hartley Suite, Building 38.

• **Social Event**

The social event dinner will be held on Tuesday, September 3\(^{rd}\), at a typical English pub (The Crown Inn) from 7:00 pm till approx. 11:00 pm.

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**Final PROGRAM**

<table>
<thead>
<tr>
<th>02.09 MONDAY</th>
<th>03.09 TUESDAY</th>
<th>04.09 WEDNESDAY</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:30</td>
<td>Registration</td>
<td>Keynote 2</td>
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<tr>
<td>9:00</td>
<td>Tutorial 1</td>
<td>Keynote 3</td>
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<tr>
<td>9:30</td>
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<td>Session 2</td>
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<tr>
<td>10:00</td>
<td>Coffee Break</td>
<td>Session 5</td>
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<td>12:00</td>
<td>Lunch</td>
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<td>12:30</td>
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<td>Panel 2</td>
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<td>13:00</td>
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<td>Session 6</td>
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<tr>
<td>13:30</td>
<td>Opening Remarks</td>
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<tr>
<td>14:00</td>
<td>Keynote 1</td>
<td>Closing Remarks/Best paper</td>
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<tr>
<td>14:30</td>
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<td>15:00</td>
<td>Coffee Break</td>
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<tr>
<td>15:30</td>
<td>Session 1</td>
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<td>16:00</td>
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<td>Coffee Break</td>
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<td>16:30</td>
<td>Session 4</td>
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<td>17:00</td>
<td>Panel 1</td>
<td>City Sightseeing</td>
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<td>17:30</td>
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<td>PhD/WiP/Poster Forum</td>
</tr>
<tr>
<td>18:00</td>
<td>Welcome Reception</td>
<td>Moving to social event</td>
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<td>18:30</td>
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<td>19:00</td>
<td>Dinner for Residentials</td>
<td>Social Event Dinner for Residentials</td>
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</tbody>
</table>

*Hands-on tutorials:*

1. Integrating ontological development with software engineering trends
2. TTool AMS extension
Monday 2

- 08:30 AM-09:00 AM Registration
- 09:00 AM-10:30 AM Hands-on Tutorial 1
  - Integrating ontological development with software engineering trends
    (Speaker: Maria Poveda Villalón and Alba Fernandez Izquierdo, Universidad Politécnica de Madrid, Spain)
- 10:30 AM-11:00 AM Coffee break
- 11:00 AM-12:30 PM Hands-on Tutorial 2
  - TTool AMS extension
    (Speaker: Daniela Genius, Sorbonne University, France)
- 12:30 PM-01:30 PM Lunch
- 01:30 PM-02:00 PM Keynote 1
  - Designing Efficient Heterogeneous Domain-Specific Languages and Compilers
    (Speaker: David Broman, KTH Royal Institute of Technology, Sweden)
- 02:00 PM-03:00 PM Session 1
  - Signal Processing and Networking
    (Chair: Julio Medina, University of Cantabria, Spain)
    - 1.1 Formal Design, Co-Simulation and Validation of a Radar Signal Processing System
      - George Ungureanu, Timmy Sundström, Anders Ahlander, Ingo Sander and Ingmar Söderquist
    - 1.2 Functional Coverage-Driven Characterization of RF Amplifiers
      - Muhammad Hassan, Daniel Grosse, Thilo Voertler, Karsten Einwich and Rolf Drechsler
    - 1.3 A methodology to compute long-term fault resilience of NoCs under fault-tolerant routing algorithms
      - Jie Hou and Martin Radetzki
- 03:00 PM-03:30 PM Coffee break
- 03:30 PM-05:00 PM Session 1
  - Systems of Systems Engineering – Where will we be in the next 20 years?
    (Moderator: Carina Zivkovic, TU Kaiserslautern, Germany)
    - Alain Girault, INRIA, Grenoble, France
    - Edward Lee, University of California Berkeley, USA
    - Scott Walker, University of Southampton, UK
- 05:00 PM-06:00 PM Panel 1
  - Systems of Systems Engineering – Where will we be in the next 20 years?
    (Moderator: Carina Zivkovic, TU Kaiserslautern, Germany)
    - Alain Girault, INRIA, Grenoble, France
    - Edward Lee, University of California Berkeley, USA
    - Scott Walker, University of Southampton, UK
- 06:00 PM-07:00 PM Welcome reception
- 07:00 PM-08:00 PM Dinner for Residents

Tuesday 3

- 08:30 AM-09:30 AM Keynote 2
  - Language Design is LEGO Design and Library Design
    (Speaker: Stephen A. Edwards, Columbia University, USA)
- 09:30 AM-11:00 AM Session 2
  - Deterministic Concurrency
    (Chair: Stephen Edwards, Columbia University, USA)
    - 2.1 Deterministic Actors
      - Edward A. Lee and Marten Lohstroh
    - 2.2 A Multi-Rate Precision Timed Programming Language for Multi-Cores
      - Alain Girault, Nicolas Hill, Eric Jenn and Eugene Yip
    - 2.3 Towards Object-Oriented Modeling in SCCharts
      - Alexander Schulz-Rosenzweig, Steven Smyth and Michael Mendler
- 11:00 AM-11:30 AM Coffee break
- 11:30 AM-01:00 PM Panel 2
  - Application of ADA Models and Languages to Industry 4.0
    (Moderator: Franco Fummi, University of Verona, Italy)
    - Frank Schirmeister, Cadence
    - Ronald Jancke, Fraunhofer IIS / EAS, Germany
    - Sara Vinco, Politecnico di Torino, Italy
    - Giulio Medina, University of Cantabria, Spain
    - Peter Wilson, University of Bath, UK
- 01:00 PM-02:00 PM Lunch
- 02:00 PM-03:30 PM Session 3
  - Modern Design Tools for Effective Property Generation
    (Chair: Heinz Rienner, EPFL, Switzerland)
    - 3.1 Syntax-Guided Enumeration of Temporal Properties
      - Gianluca Martino and Geerschwin Fey
    - 3.2 Synthesis of LTL properties from traces
      - Heinz Rienner
    - 3.3 RTL assertion mining with automated RTL to-TLM abstraction
      - Tara Ghasempouri, Alessandro Danese, Graziano Pravadelli, Nicola Bombieri and Jaak Raak
    - 3.4 Chatbot-based assertion generation from natural language specifications
      - Oliver Keßler and Ian Harris
- 03:30 PM-04:00 PM Coffee break
- 04:00 PM-05:30 PM Session 4
  - Embedded Software
    (Chair: Eugene Yip, University of Bamberg, Germany)
    - 4.1 Security Driven Design Space Exploration for Embedded Systems
      - Lucas Gressl, Christian Steger and Ulrich Neffe
    - 4.2 A Backend Tool for the Integration of Memory Optimizations into Embedded Software
      - Manuel Strobel and Martin Radetzki
    - 4.3 Timing Measurement and Control Blocks for Bare-Metal C++ Applications
      - Friederike Brunis, Kim Gruetnner and Philipp Ittenshagen
- 05:30 PM-06:30 PM PhD/WIP/Poster Forum
- 06:30 PM-07:00 PM Moving to social event
- 07:00 PM-11:00 PM Social Event

Wednesday 4

- 08:30 AM-09:30 AM Keynote 3
  - A Formal Language for Embedded Critical Software Development
    (Speaker: Marc Pouzet, École normale supérieure, France)
- 09:30 AM-11:00 AM Session 5
  - RISC-V based Firmware Design
    (Chair: Daniel Grosse, DFKI GmbH, Germany)
    - 5.1 A Context-sensitive Timing Model for Automated Firmware Generation onto RISC-V-based Microprocessor Platforms
      - Christoph Gerum, Alexander Jung, Joscha-Joel Benz, Oliver Bringmann
    - 5.2 Firmware Verification trough Concolic Testing for RISC-V Systems
      - Vladimir Hendt, Daniel Grosse, Rolf Drechsler
    - 5.3 Checking for Peripheral Device Side Effects in Firmware Variants
      - Michael Schwarz, Dominik Stoffel, Wolfgang Kunz
- 11:00 AM-11:30 AM Coffee break
- 11:30 AM-01:00 PM Session 6
  - Simulation
    (Chair: Carina Zivkovic, TU Kaiserslautern, Germany)
    - 6.1 Efficient Simulation and Parametrization of Stochastic Petri Nets in SystemC: A Case study from Systems Biology
      - Simone Caligola, Tommaso Carlucci, Franco Fummi, Carlo Laudanna, Gabriela Constantin, Nicola Bombieri and Rosalba Giugno
    - 6.2 Languages and Formalisms to Enable EDA Techniques in the Context of Industry 4.0
      - Stefano Spellini, Roberto Chirico, Michele Lora and Franco Fummi
    - 6.3 Simulation acceleration of image filtering on CMOS vision chips using many-core processors
      - Gines Domenech-Asoni and Tom Kazmierski
    - 6.4 WIP on a Coordination Language to Automate the Generation of Co-Simulations
      - Giovanni Libor and Julian Deantoni
- 01:00 PM-02:00 PM Lunch
- 02:00 PM-03:00 PM Closing remarks/Best Paper
- 03:00 PM-03:30 PM Coffee break
- 03:30 PM-07:00 PM City Sightseeing
- 07:00 PM-08:00 PM Dinner for Residents